

3.3.1.2 Output Circuit

The bytes loaded into shift registers U88 and U99 during a given horizontal time slot are shifted out by clock signal PIXCLKB during the next time slot. The resulting pixel streams, ODDBIT from U88 and EVENBIT from U99, are input to PAL U108. Here they are interleaved such that EVENBIT is displayed only during the first half of each PIXCLKB cycle and ODDBIT is displayed during the second half. Two pixels are therefore output for every clock cycle. The pixels are also logically conditioned by the attribute bits from U90. RED-ATT, GREEN-ATT, and BLUE-ATT specify the color of the "on" pixels. A low INVERSE bit reverses what is displayed for "on" and "off" pixels. A high TRANSPARENT bit allows external video to be displayed during "off" pixels.

Three video pixel streams are output from U108, one each for red, green and blue. They are buffered by open drain inverters in U104, which convert a CMOS high logic level to an analog video level controlled by VREF from I²C octal DAC U4. The resulting video signals are amplified by U105, U106 and U107 and output from the Control Module with 2X gain at 75 ohms impedance. These signals, R-INT-VID, G-INT-VID and B-INT-VID, are sent to the VIM.

Register U94 controls what the projector will display on-screen. The register is loaded by the 68000 microprocessor on the MSB of its data bus (D8-D15). Outputs W0, W1 and W2 control the width of crosshatch lines (described in section 3.2 below). The TEXTON-OFF bit turns text display off when it is low. Outputs SELECT0, SELECT1, and SELECT2 form a code determining what is displayed "behind" the text (ie. the background). These bits are input to PAL U108 for selecting between a black screen, white screen, test pattern or external video for output. Refer to Appendix C for details.

The INT-EXT signal from U108 controls fast analog switches on the VIM, which are used to switch the displayed image between internal and external video on a pixel-by-pixel basis. INT-EXT is driven high to display internal video. This allows "windows" of text (eg. a sidebar) to be overlaid onto the external video. For example, when a menu is displayed, INT-EXT is high for the part of each scan line which contains the menu, and low for the rest of the visible image.

The INT-EXT signal is also used to blank the edges of the raster. The vertical blanking signal VBL from U101 and the horizontal blanking signal HBLANK from the DPB are combined in U108 with the clamping pulse CLAMP-DP from the DPB. This creates the waveform BLANK-WFM, which is subtracted from the RGB video signals in the output amplifiers. The internal video is thus driven to black when a clamping pulse occurs and "blacker-than-black" during the remainder of the blanking intervals. At the same time, INT-EXT is driven high to display internal video, thereby blanking the display.

To prevent visible "glitching" of the image when the 68000 accesses RAM in the Character Generator, a composite blanking signal CBLANK is created in U108 and input to PAL U28. CBLANK is formed by ORing VBL and CLAMP-DP. Any access to register U94 or RAMs U97, U98 or U102 by the 68000 while CBLANK is low (ie. during active video scan) results in the insertion of wait states which delay the start of data transfer. When CBLANK goes high during a blanking interval, U28 is allowed to assert DTACK* and complete the read or write cycle. Chip selects CS-CHAR* and CS-CHARD* are likewise delayed. This prevents "glitches" on the screen which would otherwise occur when a 68000 access interrupts the transfer of pixel data from the RAMs into the shift registers. The glitches are restricted to the blanking intervals when they cannot be seen.